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10/699,764	11/03/2003	Albert Sun	MXIC 1520-1	4234

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EXAMINER	
PEERS, CHASE W	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,764	SUN ET AL.	
	Examiner	Art Unit	
	Chase Peers	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-32* is/are rejected.

7)☒ Claim(s) ~~17~~ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 17 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

The same functionality is already claimed in claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 14, and 20 rejected under 35 U.S.C. 102(e) as being anticipated by Allegrucci (Pat No 6792527).

1. Regarding claims 1, 14, and 20, Allegrucci teaches an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

The examiner notes that the CSL cells in the prior art are configuration points, but are not listed as such. The examiner also notes that although the art does not expressly cite the use of a third memory array in the memory for the configuration function, the cited paragraphs show that this limitation is still covered through the use of the MSSIU, and consequently the memory, to the CSL cells.

Furthermore, the examiner notes that other prior mentioned in this Non-Final Reject can also be used as grounds for rejection against independent claims 1 and 20. This prior art includes, two patents by Sun et al. (5901330 and 6401221).

2. Regarding claim 14, Allegrucci teaches of an interface between the processor and the configuration array that supports the configuration load function (column 2, lines 24-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-4 21-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Pani et al. (Pat No 5640344).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive

configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

Allegrucci does not disclose expressly having the memory comprises a non-volatile memory store, a floating gate memory store, or a read only memory store.

Agrawal discloses having the memory comprises a non-volatile memory store, a read only memory store (column 2, lines 6-10), or a floating gate memory store (column 10, lines 1-14).

Allegrucci and Agrawal are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the memory be a non-volatile or floating gate memory. The suggestion for doing so would have been to store data for an extended period of time without worrying about powering the memory. Therefore, it would have been obvious to combine Agrawal and Allegrucci for the benefit of storage to obtain the invention as specified in claims 1 and 20.

4. Claims 5, 6, 24 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Robb et al. (Pat No 5276839).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64) , and programmable, non-volatile memory store (column 2, lines 38-40).

Allegrucci does not disclose expressly a second store for the mission function.

Robb et al. discloses a second store for the mission function (column 3, lines 43-49).

Allegrucci and Robb et al. are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to store the mission function in memory. The suggestion for doing so would have been for easy access to the function by the processor. Therefore, it would have been obvious to combine Robb et al. and Allegrucci for the benefit of time-saving and easy access to obtain the invention as specified in claims 5, 6, 24, and 25.

The examiner notes that although it does not expressly state that the mission functions are stored on the memory, it must be noted that for the processor to do its mission for the host system, it must load the mission functions and mission data, which would come from the memory.

Claims 7, 8, 18, 19, 31, and 32 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Sun et al. (Pat No 6401221).

5. Regarding claims 7, 8, 31, and 32, Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the

configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

Allegrucci does not disclose expressly a watchdog timer coupled to the CPU, a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function.

Sun et al. discloses a watchdog timer coupled to the CPU (figure 1, item 122), a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function (column 4, lines 15-19).

Allegrucci and Sun et al. are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a watchdog timer and the functions that come with the timer. The suggestion for doing so would have been the ability to reset the system when an error occurs. Therefore, it would have been obvious to combine Sun et al. and Allegrucci for the benefit of resetting the system to obtain the invention as specified in claims 7, 8, 31, and 32.

6. Regarding claims 18 and 19, Allegrucci discloses configuration logic having configuration points to store configuration data (column 2, lines 5-23), memory storing instructions executable by the processor (column 1 line 66 to column 2 line 4), and including instructions for a configuration load function to load configuration data from an external source (column 3, lines 28-41 and column 1 line 66 to column 2 line 4).

Allegrucci does not disclose expressly error recovery during loading of the configuration data to the circuit including a processor, monitoring loading of configuration data using the configuration load function in order to detect delay in transmission of the configuration data form the remote host, restarting the configuration load function if the delay exceeds timeout, and the step of monitoring performed by using the watchdog timer on the integrated circuit and coupled to the processor.

Sun et al. discloses error recovery during loading of the configuration data to the circuit including a processor (column 2, lines 36-52), monitoring loading of configuration data using the configuration load function in order to detect delay in transmission of the configuration data form the remote host, restarting the configuration load function if the delay exceeds timeout (column 4, lines 15-19), and the step of monitoring performed by using the watchdog timer on the integrated circuit and coupled to the processor (figure 1, item 122).

Allegrucci and Sun et al. are analogous art because they are from a similar problem solving area, fault recovery on a system. At the time of the

invention it would have been obvious to a person of ordinary skill in the art to add a watchdog timer and all the functions that go along with it. The suggestion for doing so would have been system recovery in case of an error. Therefore, it would have been obvious to combine Sun et al. and Allegrucci for the benefit of system recovery to obtain the invention as specified in claims 18 and 19.

7. Claims 9, 15, and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Sun et al. (Pat No 5901330).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

Allegrucci does not disclose expressly that the configuration load function includes receiving encrypted configuration data via the input port and then decrypting the configuration data.

Sun et al. discloses that the configuration load function includes receiving encrypted configuration data via the input port and then decrypting the configuration data (column 13, lines 59-66).

Allegrucci and Sun et al. are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to encrypt the incoming data and then decrypt the data. The suggestion for doing so would have been system security. Therefore, it would have been obvious to combine Sun et al. and Allegrucci for the benefit of security to obtain the invention as specified in claims 9, 15, and 26.

The examiner notes that the in-circuit programming and the configuration load function perform the same function and are therefore not dissimilar enough to differentiate given the known definitions of the two terms.

8. Claims 10 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Lawman (Pat No 6028445).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in

configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

Allegrucci does not disclose expressly a configuration load function that includes receiving compressed configuration data via an input port and then decompressing the data.

Lawman discloses a configuration load function that includes receiving compressed configuration data via an input port and then decompressing the data (column 8, lines 12-33).

Allegrucci and Lawman are analogous art because both deal with downloading data in a compressed format to a programmable device. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow the configuration load function to receive compressed data and to decompress it. The suggestion for doing so would have been to save time and

bandwidth. Therefore, it would have been obvious to combine Lawman and Allegrucci for the benefit of time and bandwidth savings to obtain the invention as specified in claims 10 and 27.

9. Claims 11-13 and 28-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Trimberger (Pat No 6105105).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

Allegrucci does not disclose expressly the configuration points comprising either floating gate memory cells, non-volatile charge programmable memory cells, or non-volatile programmable memory cells.

Trimberger discloses the configuration points comprising either floating gate memory cells, non-volatile charge programmable memory cells, or non-volatile programmable memory cells (column 4, lines 12-21).

Allegrucci and Trimberger are analogous art because they are both processing systems that employ reconfigurable programmable logic. At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the configuration points comprise floating gate or non-volatile memory cells. The suggestion for doing so would have been to make sure the data can survive a loss of power or reset to the system. Therefore, it would have been obvious to combine Trimberger and Allegrucci for the benefit of not losing data to obtain the invention as specified in claims 11-13 and 28-30.

10. Claim 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci as applied to claim 1 above, and further in view of Akao et al. (Pat No 5900008).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic (column 2, lines 5-23), a memory to store instructions executable by the CPU (column 1 line 66 to column 2 line 4), storing instructions for the configuration load function used to receive

configuration data via the input port, storing instructions for the configuration load function used to transfer configuration data to the configuration logic array, storing instructions in a second memory array of said memory for the configuration load function used to receive configuration data from an external source, storing instructions in a third memory array for the configuration function used to transfer configuration data to programmable configuration points in the configuration logic (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), configuring an integrated circuit including a processor, a processor coupled to memory which executes instructions from memory (column 2, lines 55-64).

Allegrucci does not disclose expressly having the memory include a protected memory array storing instructions for a first configuration load function, a second memory array storing instructions for a second configuration load function, the first memory array protected from alteration by a programming function, and the second memory accessible to be written/modified by the programming function.

Akao et al. discloses having the memory include a protected memory array storing instructions for a first configuration load function, a second memory array storing instructions for a second configuration load function, the first memory array protected from alteration by a programming function, and the second memory accessible to be written/modified by the programming function.

Allegrucci and Akao et al. are analogous art because they are from a similar problem solving area, processing systems that employ program areas and protection for some of the areas. At the time of the invention it would have been

obvious to a person of ordinary skill in the art to add a protected memory area. The suggestion for doing so would have been protect the data from accidental or malicious overwrites/deletes. Therefore, it would have been obvious to combine Akao et al. and Allegrucci for the benefit of data protection to obtain the invention as specified in claim 16.

The examiner notes that Akao et al. does not expressly state protecting the first configuration load function or not protecting the second configuration load function, but that combining Akao et al. and Allegrucci would give anyone with skill in the art motivation to protect one of the configuration load functions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chase Peers whose telephone number is (571) 272-6757. The examiner can normally be reached on from Monday to Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
12\23\05